ECCentric: An Empirical Analysis of Quantum Error Correction Codes

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Quantum Error Correction (QEC) is essential for building scalable quantum computers, but a lack of systematic, end-to-end evaluation methods makes it difficult to assess how different QEC codes perform under realistic conditions. The vast diversity of codes, an expansive experimental search space, and the absence of a standardized framework prevent a thorough, holistic analysis. To address this, we introduce ECCentric, an end-to-end benchmarking framework designed to systematically evaluate QEC codes across the full quantum computing stack. ECCentric is designed to be modular, extensible, and general, allowing for a comprehensive analysis of QEC code families under varying hardware topologies, noise models, and compilation strategies.

Using ECCentric, we conduct the first systematic benchmarking of major QEC code families against realistic, mid-term quantum device parameters. Our empirical analysis reveals that intra-QPU execution significantly outperforms distributed methods, that qubit connectivity is a far more critical factor for reducing logical errors than increasing code distance, and that compiler overhead remains a major source of error. Furthermore, our findings suggest that trapped-ion architectures with qubit shuttling are the most promising near-term platforms and that on noisy devices, a strategic and selective application of QEC is necessary to avoid introducing more errors than are corrected. This study provides crucial, actionable insights for both hardware designers and practitioners, guiding the development of fault-tolerant quantum systems.

CCS Concepts: • **Hardware** → **Quantum error correction and fault tolerance**; Quantum technologies; • **Computer systems organization** → **Quantum computing**; • **General and reference** → *Evaluation*; *Empirical studies.*

Additional Key Words and Phrases: quantum computing, quantum error correction, benchmarking

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1 Introduction

Context and motivation. While the promise of quantum computing [9, 58, 101, 118] has led to the rapid development and accessibility of Quantum Processing Units (QPUs) [11, 12, 56, 71, 105, 107], achieving true quantum advantage is fundamentally limited by persistent hardware noise [101].

Quantum Error Correction (QEC) offers the only known path to fault tolerance, a prerequisite for building scalable quantum computers capable of solving classically intractable problems [4, 46, 52]. It encodes a single logical qubit into a redundant, entangled system of multiple noisy physical qubits [98, 101]. Once such an encoded circuit is transpiled into the hardware's native gate set and

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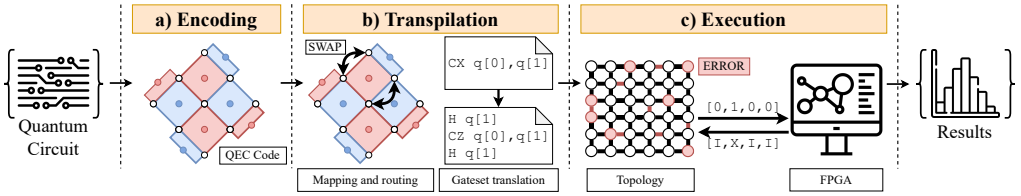


Fig. 2. Workflow of a quantum circuit protected with QEC, showing how mapping and routing, translation, and decoding are handled during execution.

adapted to its topology (Fig. 2), it is executed on the device, where syndrome measurements are continuously performed, allowing the decoder to correct errors in real time [16].

Notably, a diverse family of QEC codes exists, each with unique resource overheads, operational assumptions, and performance characteristics. Their suitability heavily depends on the underlying physical qubit technology and its noise model [26, 46].

Research gap and challenges. Despite the variety of QEC codes, there's a significant research gap: a lack of a systematic, end-to-end methodology for rigorously comparing them. This makes it challenging to accurately assess a code's performance under the specific, realistic noise and software constraints of a particular QPU. A comprehensive practical evaluation needs to consider the entire execution pipeline, as each stage can influence the code's effectiveness.

Unfortunately, current QEC evaluations are often ad hoc and limited, either focusing on a small number of codes with oversimplified noise models [36, 45, 67, 69] or analyzing components such as decoders in isolation [17, 32, 37, 43, 60, 82, 127, 139]. As a result, no existing benchmarking framework provides an end-to-end, systematic evaluation. Current tools exhibit a distinct dichotomy: fast, specialized simulators, such as Stim [49], are hardware-agnostic and rely on simplistic error models, whereas general-purpose frameworks, such as Qiskit [73], lack the scalability needed to simulate large, fault-tolerant codes [46]. These limitations create a major blind spot in practical quantum computing.

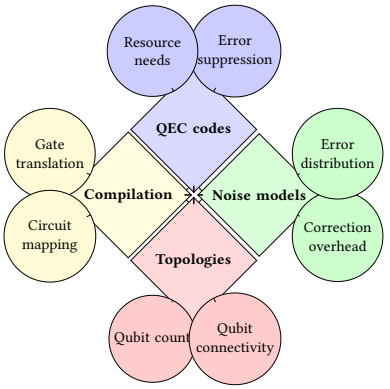


Fig. 1. Our comprehensive framework provides a structured empirical analysis of QEC landscape. We examine the QEC field across four key dimensions, addressing eight critical research questions.

To effectively address this research gap, we must confront three fundamental challenges. *Firstly, the diverse QEC landscape:* A vast number of codes exist, each with unique overheads, error thresholds, and decoding complexities, making it difficult to compare their effectiveness across different hardware and noise models [24, 33, 37, 74, 129, 135]. *Secondly, the vast experimental search space:* A code's performance is determined by a multi-dimensional interplay of QPU topology, physical noise, and compiler artifacts, rendering an exhaustive search computationally intractable [18, 127, 134, 136]. *Finally, the lack of a suitable benchmarking framework:* Existing tools are either too slow for large-scale studies (e.g., Qiskit [73]) or too hardware-agnostic for realistic evaluation (e.g., Stim [49]). A viable solution must be general, supporting a wide spectrum of code families and QPU architectures; extensible, to easily integrate new decoders and evolving noise models; and modular, to enable the isolation and analysis of specific stages within the QEC pipeline, from encoding to decoding.

Research question and our approach. These challenges lead to our central research question: *How can we systematically evaluate the suitability of quantum error correction (QEC) codes for practical applications on current and near-term quantum devices?*

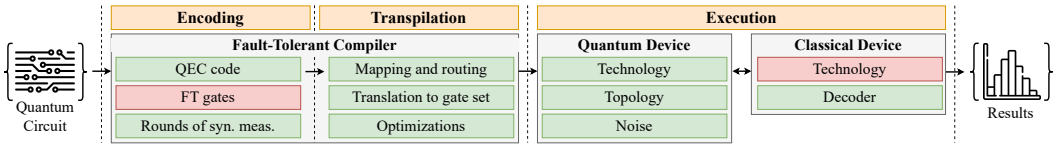


Fig. 3. Lifetime of a quantum circuit protected with QEC code. *Our analysis covers the elements in green.*

To answer this question, we propose a two-staged approach. First, we impose structure on the diverse and rapidly evolving QEC landscape by creating a systematic taxonomy of QEC codes. From this taxonomy, we have identified five primary families of codes and selected a representative member from each to ensure our analysis is both fair and comprehensive.

Building on this foundational taxonomy, we introduce ECCentric, a new, end-to-end benchmarking framework designed for the systematic evaluation of QEC codes on current and near-term quantum devices. ECCentric is general, capable of supporting a wide array of QEC codes, QPU technologies, and compiler back-ends. It is modular, allowing researchers to customize the evaluation pipeline and scope of their experiments. And it is extensible, making it easy to integrate new code, hardware features, and compilation strategies as they emerge.

Leveraging the full capabilities of the ECCentric framework, we structure our investigation around four key dimensions (presented in Fig. 1) that influence QEC performance, defining two targeted research questions for each to systematically assess their impact. These four dimensions include *QEC codes*, where we select six representative codes from all major families using our QEC code taxonomy; *QPU noise models*, where we include both ideal and realistic models derived from current (e.g., Google Willow [3]) and next-generation (e.g., Quantinuum Apollo [105] and IBM Flamingo [107]) quantum devices; *QPU topologies*, where we explore a range of layouts, from abstract to the complex architectures of existing hardware (e.g., Google Willow [3] and Inflection [111]), varying qubit count and connectivity to isolate the impact of topology; and finally, *quantum compilation*, where we investigate how different quantum compilers (e.g., Qiskit [73] and TKET [120]) and their internal stages, such as mapping and routing heuristics (e.g., SABRE [88]), affect QEC performance.

Our key findings, implications, and lessons learned. Our systematic evaluation reveals several critical insights and implications for both hardware and software development:

- *Fault-tolerance with Trapped-Ion is near:* Our analysis of projected hardware roadmaps shows that the planned error rates and qubit shuttling capabilities of these devices should eliminate logical errors across most evaluated codes within the next five years [105].
- *Intra-QPU execution is superior:* Our results show that distributing codes across QPUs increases the logical error rate by 69.14% compared to single-QPU execution. However, while link fidelity is a factor, the principal issue is the low number of connections, and hardware development should prioritize increasing the cross-QPU links rather than solely focusing on their fidelity.
- *Prioritize connectivity over code distance:* Our experiments show that increasing code distance is often ineffective, increasing the logical error rate on average by 0.012 with only 30.95% of adjustments yielding meaningful improvement. In contrast, improving connectivity provides substantial gains: moving from a grid to a fully connected topology reduces the logical error rate by 81.9%, while devices with qubit shuttling outperform those without by 45.48%. Thus, hardware manufacturers should prioritize improving qubit connectivity.
- *QEC-aware compilation is essential:* The compilation process introduces significant overhead that can undermine the benefits of error correction. We find that mapping and routing add an average of 134.095% more two-qubit gates, while optimized translation still adds 3.166 extra gates per original gate. Mitigating this requires QEC-aware compilers that optimize at the logical-qubit

Table 1. Overview of quantum technologies. *Quantinuum (Q.) Apollo [105] data are extrapolated from H2 device specifications [106]. For Infleqtion, reset error is included in readout error, leakage in gate error, and SPAM is approximated as measurement plus reset, as it is not directly reported [111].*

Characteristic	**Superconducting**		**Trapped-Ion**	**Neutral Atoms**
Qubit Type	Transmon qubits [114]		Trapped ions [28]	Rydberg atoms [62]
Topology	heavy-hex [107], grid [3]		race track [96], grid [105]	2D array [111] arbitrary 3D geometry [15]
Mid-Circuit Qubit Movement	No		Yes [96]	Yes [19]
Coherence Time	10 - 100 μs [81]		> 4s [105, 130]	1 - 60s [132]
Operation Speed	12 - 25 ns [10]		1-10 μs [116]	0.4 - 2 μs [132]
Real Error Rates	**Willow** [3]	**Flamingo** [2]	**Q. Apollo** [105, 106]	**Infleqtion** [111]
SQ	6.2×10^{-4}	2.5×10^{-4}	8.0×10^{-6}	9.8×10^{-4}
2Q	2.8×10^{-3}	2.0×10^{-3}	1.4×10^{-4}	6.5×10^{-3}
SPAM	9.5×10^{-3}	2.5×10^{-4}	1.33×10^{-4}	4.0×10^{-3}
Idle	9.0×10^{-3}	-	5.3×10^{-5}	-
Crosstalk	5.5×10^{-4}	-	6.3×10^{-7}	-
Leakage	2.5×10^{-4}	-	4.3×10^{-5}	-

level, for example, by prioritizing efficient routing to busy ancilla qubits and canceling redundant gate sequences across repeated QEC cycles.

- *Heterogeneity is not a primary concern:* We find the variability in individual qubit quality or in readout correctness has a negligible impact on performance, changing the logical error rate by 0.02 on average. This suggests that complex, variance-aware compilation strategies might be an unnecessary burden. This frees compiler developers to de-prioritize these intricate techniques and instead pursue more straightforward and effective designs.
- *Apply QEC strategically, not universally:* On noisy, near-term devices, the indiscriminate application of QEC can be counterproductive. Our results show that at a physical two-qubit error rate of 0.002, most of our evaluated codes fail, and at 0.004, none remain effective, introducing more errors than they correct. This necessitates a selective approach where QEC is only used for operations or qubits where its benefits outweigh its overhead.

Our contributions. Overall, to the best of our knowledge, this paper provides the first systematic benchmarking of multiple QEC codes, focusing on their practical application on real-world hardware, compilers, and noise models. Our contributions are summarized as follows:

- *Experimental QEC code analysis:* A systematic benchmarking of the major Quantum Error Correction (QEC) code families under realistic experimental conditions.
- *ECCentric framework:* The design of a modular benchmarking framework that can be readily extended to incorporate additional codes, devices, noise models, and decoders.
- *QEC code taxonomy:* The introduction of a structured taxonomy for QEC codes, clearly presenting the differences and shared characteristics among the primary families.
- *Concatenated Steane code extension:* The first extension of the [[49,1,9]] concatenated Steane code [99] to [[373,1,27]] concatenated Steane code.

2 Quantum Error Correction (QEC)

QEC is a technique of protecting quantum information from noise by encoding it into entangled states of multiple qubits, i.e., logical qubits [98]. Preparing and running such protected circuits, however, requires a complex toolchain that extends well beyond standard compilation. To the best of our knowledge, no fully integrated end-to-end compiler for QEC exists, but building on existing frameworks [84, 131], we illustrate in Fig. 3 the stages of compiling and executing a quantum circuit with QEC, each of which can introduce overhead and weaken protection:

Encoding. To provide protection for a quantum circuit (Fig. 2(a)), we start by choosing a QEC code matching the constraints of the device regarding topology and noise profile, and preparing logical qubits by entangling them with themselves and with ancilla qubits accordingly. Next, we translate the gates in the circuit into fault-tolerant (FT) gates able to manipulate logical qubits without falsely marking errors [98]. While some gates can be translated with relatively low overhead, they alone cannot form a universal set [40]. Missing gates need to be added with costly techniques such as code switching [8], lattice surgery [65], or magic state distillation [25]. At present, no general tool can automatically translate an arbitrary circuit into a fully encoded form with support for these gates. Afterwards, we insert rounds of syndrome measurement periodically into the circuit, i.e., additional stages of measurement done on the ancilla qubits entangled with data qubits, which detect whether errors have occurred [98].

Transpilation. Now we need to adapt the circuit to the target device [93]. Transpilation involves multiple stages [7, 78, 109]: Firstly, we map the logical qubits of the circuit to physical qubits of the device on which they will be executed [89]. To make two-qubit gate execution possible, qubits involved in them need to be placed on physically adjacent hardware. However, as that is not always possible, we follow this stage with routing, during which we insert a gate sequence (typically an additional swapping operation) to move together the quantum states that must interact [136]. To keep overhead low, we aim for routing sequences that minimize the number of movements. We then translate each gate in the circuit into an equivalent operation from the elementary set supported by the target device [48], as we illustrate in Fig. 2(b). Since mapping the large connection graph, inserting SWAP operations, and decomposing unsupported gates produce substantial overhead, we interleave those mandatory stages with optimization passes, which aggressively prune the length and the gate count of the circuit [76], e.g., by removing mutually cancelling gates.

Execution. The promise of quantum computing [58, 119] has spurred the development of diverse hardware platforms [28, 62, 68], each with distinct trade-offs in coherence times, gate speed, connectivity, and noise profiles, as summarized in Tab. 1. Superconducting devices, the most common platform, offer fast gates but are constrained by limited qubit lifetimes and fixed, sparse connectivity, making them particularly susceptible to idling errors, crosstalk between neighboring qubits, and more gate errors introduced by additional SWAP operations [3, 68]. In contrast, trapped-ion and neutral atoms devices provide longer coherence and can achieve dynamic, all-to-all connectivity via mid-circuit qubit movement, but are affected by errors arising from qubit transport and imperfect control lasers [19, 28, 96, 111, 130]. Each platform's unique error characteristics are a critical factor for the effectiveness of QEC [32].

During circuit execution, those errors can prevent us from obtaining meaningful results. To handle them, we periodically take syndrome measurements and send the results to a classical processor, commonly an FPGA [90] or GPU [44], where a decoder, usually tailored to the chosen QEC code, locates errors and selects the appropriate corrections, trading off precision and speed to apply them before qubits decohere [16]. The performance depends on the specific combination of QEC code, decoding algorithm, and hardware, especially regarding latency. This process, which we illustrate in Fig. 2(c), is essential to suppress noise and ultimately enable effective circuit execution.

Table 2. Research questions we pursue in this work, their relations to the considered problem dimensions, and the sections where they are discussed.

Sec.	Research Question	Codes	Topologies	Noise	Compilation
§4	**RQ#1**: Will the effectiveness of the QEC codes noticeably change when their distance expands?	✓	✓	✗	✗
	RQ#2: Does higher qubit connectivity always improve the effectiveness of QEC codes?	✓	✓	✗	✓
	RQ#3: Does qubit quality variance critically impact logical error rates beyond the effect of the mean?	✗	✗	✓	✓
	RQ#4: Does a QEC code's performance scaling differ between single-QPU and distributed execution?	✓	✓	✗	✗
	RQ#5: Which quantum technology provides favorable error rates and hardware features for effective QEC?	✓	✓	✓	✗
§5	**RQ#6**: How do mapping and routing compilation stages influence the effectiveness of QEC codes?	✓	✗	✗	✓
	RQ#7: How does the translation stage influence the effectiveness of QEC codes?	✓	✗	✗	✓
§6	**RQ#8**: Which decoders achieve the best performance across QEC code families?	✓	✗	✓	✗
	RQ#9: Is applying QEC always beneficial, or can the QEC overhead become a net source of error?	✓	✗	✓	✗

Takeaway: Effective QEC performance depends on the entire quantum computing stack, as every stage from compilation to execution introduces potential overhead and errors. *First*, encoding and translation decisions, such as the frequency of syndrome measurements and the conversion to fault-tolerant gates, create significant qubit and gate overhead [61, 85]. *Second*, the transpilation of large QEC circuits adds substantial routing overhead, with each extra gate introducing more noise that degrades the code's effectiveness [42, 100]. *Last*, the hardware and decoder are critical; a device's topology and noise profile determine a code's viability, while a slow or inaccurate decoder can introduce more errors than it corrects [18, 37, 127].

3 Overview

In this section, we discuss the scope of our study along with its limitations and introduce the research questions we aim to address (§ 3.1). Then, we present a systematic taxonomy of QEC codes to enable their methodical exploration (§ 3.2). Finally, we propose our novel benchmarking framework (§ 3.3), which we later use for the experimental evaluation (§ 4, § 5, § 6).

3.1 Research Scope

Each of the steps introduced in § 2 requires in-depth exploration to evaluate its impact on error correction. Taken together, these steps create a combinatorial explosion of factors, making exhaustive analysis infeasible within a single study. To manage this complexity, we slightly narrow the scope. We exclude the construction of FT logical gates, as, to the best of our knowledge, the only existing framework supporting them is limited to the surface code and still under active development [1], and developing a general, scalable FT gate constructor would constitute a substantial standalone contribution. FT gates would require far more resources and greatly increase circuit depth, resulting in higher logical error rates. We also omit classical decoder latency, which depends strongly on the code, decoder, and hardware platform, making any arbitrary artificial value unsuitable for general analysis. Since real-time decoding is planned to operate under 1 μs, the resulting decoherence errors in a real system would be only marginally higher than those observed here [16]. We further discuss both limitations in § 7. Additionally, because circuit optimization techniques generally

improve performance by reducing gate overhead, we treat them as a secondary consideration during compilation.

Even with these restrictions, the remaining scope remains substantial. To approach it systematically, we organize our work around four key dimensions: QEC codes, quantum compilation, quantum device noise models, and quantum device topology. Based on these dimensions, we formulate nine research questions, summarized in Tab. 2, which probe their impact on QEC effectiveness. We select these questions to ensure comprehensive coverage while focusing on practical aspects of compilation and execution, reflecting current development directions and targeting well-known bottlenecks (e.g., limited device size or transpilation overhead). By addressing them experimentally, we aim to generate practical insights that guide real-world QEC implementations.

3.2 Quantum Error Correction Codes Taxonomy

To enable a fair and systematic evaluation across the vast landscape of QEC codes, we first introduce a taxonomy to structure our analysis. As shown in Tab. 3, we organize codes into four main families based on their core principles: subsystem stabilizer, QLDPC, concatenated, and topological codes. We describe each family through its core principles and highlight important variations where relevant:

Table 3. Taxonomy of main QEC code families.

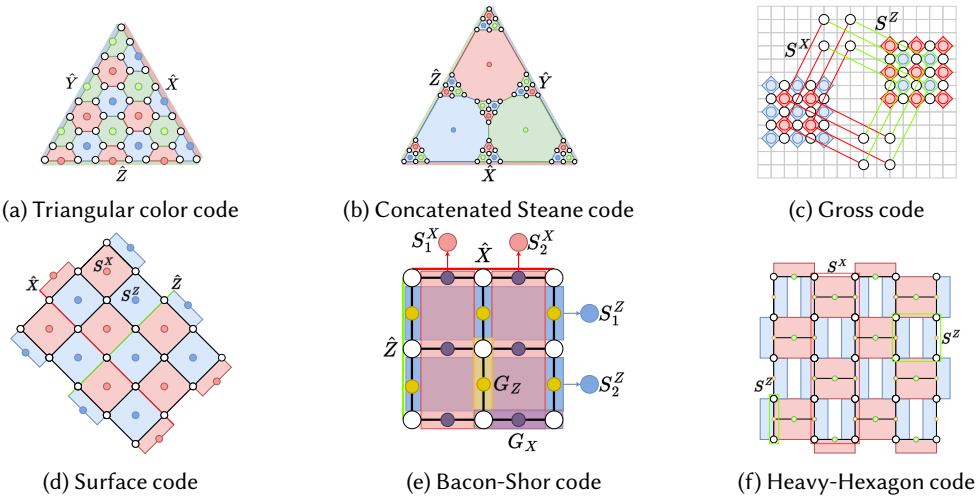
Subsystem			
Stabilizer			
Concatenated	**QLDPC**	**Topological**	**Subsystem Stabilizer**
Concatenated Steane	BB (Gross)	Surface, Color	Bacon-Shor
		Heavy-hex	

Stabilizer codes. Stabilizer codes are built upon a group of mutually commuting Pauli operators $\mathcal{S}$, where a state $|\psi\rangle$ satisfies $S|\psi\rangle = |\psi\rangle$ for all $S \in \mathcal{S}$ [57]. Errors are detected through syndrome extraction: data qubits are entangled with ancillas prepared in known states, which are then measured to reveal occurring errors [112]. Their compatibility with efficient classical simulation has made stabilizer codes the foundation of most QEC schemes.

To describe specific code instances of stabilizer codes, we use the standard $[[n,k,d]]$ notation, where n is the number of physical qubits used to encode k logical qubits, and d is the code distance, which is the minimal number of physical qubits that must be corrupted before an error becomes undetectable [112]. Notably, n does not include ancilla qubits required for syndrome measurement.

Subsystem stabilizer codes. Subsystem codes generalize stabilizer codes by encoding logical information into a subsystem instead of a subspace, introducing additional degrees of freedom, called gauge qubits, which do not influence the logical information and can be viewed as non-essential bits [6]. In practice, attention centers on the *subsystem stabilizer* subclass, which preserves the stabilizer formalism for efficient simulation while using gauge operators to replace some stabilizers with lower-weight checks, simplifying syndrome extraction [63]. An example of a subsystem stabilizer code is the *Bacon-Shor code* [13]. Defined on a rectangular lattice of size $m_1 \times m_2$, it has parameters $[[m_1 m_2, 1, \min(m_1, m_2)]]$ [41], and is particularly well-suited for trapped-ion devices, where under realistic noise models it can outperform the state-of-the art code with larger distance [38].

Topological codes. Topological codes encode information in global features of a lattice, making them intrinsically robust against local errors [21, 79]. Their local stabilizers correspond to lattice features like vertices or plaquettes, and their distance grows with the lattice size. Among topological codes, *surface codes* [46] are the most studied and considered as state-of-the-art [140], typically defined on a 2D square lattice. A prominent variant, the *rotated surface code*, reduces the physical qubits overhead [66] while preserving the code's core properties. Another key subclass is *color codes* [22], defined on lattices with colored plaquettes so that no two adjacent plaquettes share the same color, with each color corresponding to a subset of stabilizers. A notable example is the *triangular color code*, built on a 6.6.6 hexagonal lattice with three plaquette colors, which combines strong



(a) Triangular color code (b) Concatenated Steane code (c) Gross code

(d) Surface code (e) Bacon-Shor code (f) Heavy-Hexagon code

Fig. 4. Visualization of the six QEC codes explored in this work. *White dots represent data qubits, yellow and purple dots indicate gauge qubits, and remaining dots correspond to additional ancilla qubits.* $\hat{X}$, $\hat{Y}$, *and* $\hat{Z}$ *symbolize logical operators,* G_X *and* G_Z *gauge operators. Field colors indicate stabilizers* S^X *and* S^Z.

error suppression with a versatile set of low-overhead fault-tolerant gates, making it a promising candidate for scalable quantum computing [21, 83].

Quantum low-density parity-check (QLDPC) codes. QLDPC codes are stabilizer codes with sparse parity-check matrices, meaning that each stabilizer involves only a small subset of qubits [26]. This sparsity reduces measurement complexity but at the cost of long-range connectivity. The key advantage of QLDPC codes lies in their efficient scaling, maintaining a constant logical-to-physical qubit ratio (encoding rate) as the code distance grows. A prominent subclass of QLDPC codes is *bivariate bicycle (BB) codes* [24], which are constructed from bivariate polynomials with regular stabilizer patterns, preserving a good encoding rate while achieving even higher physical error rates they can tolerate (error thresholds). A notable example is the *gross code* [[144,12,12]], which encodes 12 logical qubits using 288 physical qubits, achieving performance comparable to a surface code that would require thousands of qubits [24].

Concatenated codes. Concatenated codes encode quantum information by nesting one code within another [80]. Specifically, an outer code encodes the logical qubits, and each physical qubit of this code is further encoded using an inner code. This layered structure allows flexible combinations of codes to improve error correction. A notable example of a concatenated code is the *concatenated Steane code* [99], denoted as $[[7^m,1,3^m]]$, able to achieve even lower logical error rates than the triangular color code. It is constructed by recursively concatenating the standard Steane code [[7,1,3]] [121] with itself $m-1$ times. However, a common drawback of concatenated codes is that their encoding rate decreases exponentially with the concatenation level.

Architecture-specific codes. Additionally, although we do not distinguish them as a family, some QEC codes are designed to combine different characteristics to meet the constraints of specific quantum hardware. A prominent example is the *heavy-hexagon code*, introduced as a sparse alternative to the surface code [31] and developed for the heavy-hex topology (e.g., IBM Heron [2]). It blends topological features, using a lattice-based layout, with subsystem stabilizer properties, leveraging gauge operators to reduce qubit connectivity.

For our study, we select representative codes from each major family: the Bacon-Shor, rotated surface, triangular color, gross, and concatenated Steane codes, each chosen as a high-performing

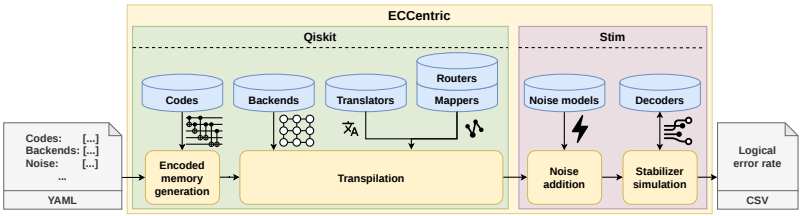


Fig. 5. Architecture of the ECCentric framework. *Our design of a fully modular and extensible setup, enabling systematic study of the different aspects of QEC realization.*

exemplar of its category. We specifically include both the state-of-the-art surface code and the color code, as the latter has promising properties for practical implementations. Additionally, we include the heavy-hex code to test how a topology-specific code performs under general conditions. The structures of these codes are illustrated in Fig. 4.

3.3 The ECCentric Framework

To experimentally explore our research questions while systematically exploring the important parameters, we now require a high-performance and modular framework that incorporates different compilation stages, topology constraints, and detailed noise models. However, existing tools either support detailed compilation and execution (e.g., Qiskit [73]) or are fast and memory-efficient enough for QEC simulation (e.g., Stim [49]), with no single framework fully meeting our needs. To address this gap, we develop ECCentric, our dedicated, fully modular, extensible framework for systematic evaluation of the QEC codes, which we present in Fig. 5.

Encoded quantum memory generation. We first use pre-existing libraries [49–51, 55, 86, 99] to generate quantum memory circuits, i.e., circuits representing one or more logical qubits encoded using our selected codes, not supporting FT logical gates, as discussed in § 7. Generation allows arbitrary error-correction rounds and flexible code distance. For the surface, color, Bacon–Shor, and heavy-hex codes, we only generate odd-distance instances to avoid overhead or complications from majority-voting syndrome extraction [27, 30, 46], while the gross code has a fixed distance of 12 [24]. We further extend the Steane code with an additional concatenation layer to produce a [[343,1,27]] code and provide it at distances 3, 9, and 27. We generate all circuits in the Stim format [49] and subsequently translate them into Qiskit [73] to enable execution.

Translation. Next, circuits are transpiled to the native gate sets of target devices using high-performance translators, including Qiskit [73], TKET [120], and BQSKit [137] translators, selected for their performance [97]. By default, we only use the translation functionalities of these SDKs. For full simulation, the circuits must conform to the gate set supported by Stim, so we perform an additional translation during the mapping and routing stage to guarantee that any gates not supported by Stim are correctly converted before execution.

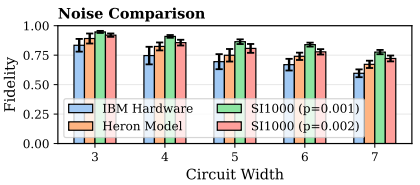


Fig. 6. Comparison of real hardware, the Heron noise model, and standard artificial noise models. *Greater similarity to hardware indicates a more realistic model. We run 10 circuits per width with 1000 shots and report mean fidelity relative to a noiseless simulation.*

Mapping and routing. We define all backends as custom artificial devices based on Qiskit's BackendV2 [73], specifying their topology and, where applicable, qubit properties, such as T_1 and T_2 times. We support both synthetic topologies and models of real devices: Google Willow [3], Quantinuum Apollo [105], Infleqtion [111], IBM Flamingo [107], and IBM Nighthawk [108]. To enable execution of codes, we scale some devices up to reflect mid-term projections, such as Google Willow (3×,

315 qubits) and Infleqtion (16×, 384 qubits), while limiting others like Apollo to 768 qubits for simulation feasibility.

For devices supporting mid-circuit movement, we model shuttling by adding temporary, full-connectivity links with distinct durations and error rates to represent a qubit moving to its target for a remote gate and then returning. We then use the Qiskit Transpiler [109] to determine the initial layout and perform routing while also exploring all available parameters: the initial layout strategies ("Trivial," "Dense," "Lookahead," and "Sabre") and routing algorithms ("Basic," "Stochastic," and "Sabre"). We also implement a qubit tracker to maintain the mapping between physical and logical qubits throughout the circuits, to ensure accurate noise modeling throughout this process.

Representation change. To enable efficient stabilizer simulation, we translate the circuits into the Stim format. Since Qiskit circuits do not include Stim-specific gates (e.g., MRX), we represent these operations as sequences of standard gates in the resulting Stim circuits. We verify the correctness of this translation both manually and automatically across a range of code samples.

Noise addition. After translation, we inject noise gate-by-gate to ensure compatibility with our stabilizer simulation. Our framework supports ① single- and two-qubit gate errors, ② idle errors (modeled either with a constant probability or derived from qubit-specific T_1/T_2 times and gate durations), ③ leakage with propagation, ④ crosstalk, ⑤ reset errors, ⑥ readout errors, ⑦ qubit shuttling errors (modeled as decoherence proportional to movement time [20]), and ⑧ inter-chip gate errors, extending the approach of [54]. We provide both standard models, such as a modified SI1000 [54], and realistic, device-specific models for platforms including Infleqtion, Google Willow, IBM Flamingo, and Quantinuum Apollo (Tab. 1). Fig. 6 illustrates how closely our framework can approximate an actual device.

Stabilizer simulation. Finally, we run a stabilizer simulation using Stim [49], which tracks only the stabilizers rather than full quantum states, allowing efficient, exact simulation without approximations, to sample how physical errors propagate and which syndromes they trigger. We compile these samples into detector error models [39] and feed them to a decoder, which infers the most likely error pattern and applies corrections. We provide two general-purpose decoders: minimum-weight perfect matching (MWPM) [64] and belief propagation with order statistic decoding (BP-OSD) [113], selected for their effectiveness across all codes we study and their well-established open-source implementations. We describe the decoders and justify our choices in more detail in Appendix 6.1. The logical error rate is then estimated as the fraction of runs where errors remain uncorrected.

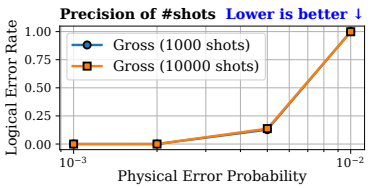


Fig. 7. Effect of the number of shots on logical error rate precision. *Logical error rate of the gross code under the SI1000 noise model for 1000 and 10000 shots.*

Experimental setup. Unless stated otherwise, we use circuits at the maximal code distance supported by the topology, with a number of error-correction rounds equal to the code distance. We run each experiment for 1000 shots, giving confidence intervals of ≈0.004 for logical error rates expected at error probabilities around 0.004, which are at most this value in low-error regimes, while higher rates indicate code failure. This shot count is sufficient to distinguish these regimes and assess the suitability of each code without incurring high computational cost. In Fig. 7, we show that for the gross code, which has the most gates and therefore experiences more opportunities for errors, the logical error rates for 1000 and 10000 shots overlap, indicating that 1000 shots already provide sufficient statistical resolution across this error range.

Table 4. Ratio of logical to physical qubits and number of two-qubit gates based on our implementations of the QEC codes. *Distance 11 for the majority of codes, 12 for the gross code, and 9 for the concatenated Steane with 3 syndrome measurement rounds.*

	Surface	Bacon-Shor	BB (Gross)	C. Steane	Color Code	Heavy-Hex
Net Enc. Rate	$\frac{1}{2d^2-1}$	$\frac{1}{d^2}$	$\frac{k}{2n}$ $(\frac{1}{24})$ [24]	$\frac{1}{2\cdot 7^m}$	$\frac{4}{(3d-1)^2}$ [30]	$\frac{2}{(5d^2-2d-1)}$ [31]
#Phys. Qubits	274	121	288	98	181	291
#2Q	1320	1320	2592	961	1440	1920

4 Hardware Restriction Analysis

In this section, we present a detailed effectiveness analysis of the chosen QEC codes across the hardware-related dimensions: topology size (§ 4.1), topology connectivity (§ 4.2), variance of qubit quality (§ 4.3), distributed device (§ 4.4), and different realistic quantum technologies (§ 4.5).

4.1 Topology Size

We examine how the performance of QEC codes scales with the number of physical qubits. The scale of quantum hardware is rapidly increasing, with roadmaps projecting growth from hundreds of qubits on current devices, such as Google's Willow [3] and IBM's Flamingo [107], to thousands on future Quantinuum systems [105]. This expansion in qubit count enables the usage of larger codes. Conventionally, a larger code distance is expected to yield superior error suppression, as it directly determines the maximum number of correctable errors [112]. Tab. 4 lists the encoding rate of each code, and Fig. 8 shows the maximum possible distance for the Surface and Bacon-Shor codes on devices with 20, 40, and 60 qubits.

Research question and hypothesis. This leads to the question: **RQ# 1**: *Does a QEC code's effectiveness change as its distance increases?* Our hypothesis is that a higher distance is always more beneficial, and thus, the decision on how many qubits to use will lead to a trade-off between using the entire QPU for the best protection of one qubit or having more qubits under less severe protection. Fig. 8 illustrates a key resource trade-off using a 60-qubit device. With the surface code, one could implement a single distance-5 patch or three distance-3 patches. With the Bacon-Shor code, the options include one distance-7 patch, two of distance-5, or six of distance-3.

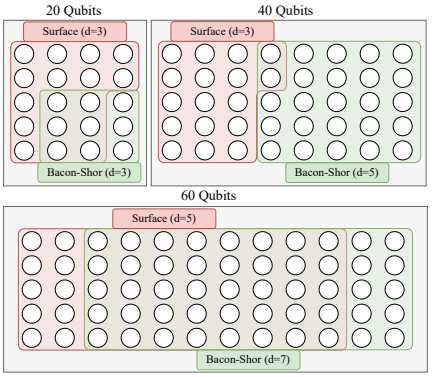


Fig. 8. QEC codes possible on different device sizes. *An overview of the attainable distances for the surface code (in red) and the Bacon–Shor code (in green) on systems with 20, 40, and 60 qubits.*

Methodology. To investigate this trade-off, we simulate our selected QEC codes with 1000 shots at their maximum possible distance, corresponding to the distance number of rounds on an idealized, all-to-all connected 300-500 qubit backend. For comparison, we include the fixed-distance gross and concatenated Steane ([[49,1,9]]) codes as baselines. The simulations employ two error models: the SI1000 model and a more severe uniform error model with an error probability of 0.004.

Results. Our results in Fig. 9 show that a code's distance provides surprisingly little benefit. We observe no consistent improvement with distance; a larger distance on average corresponds to a slight increase in the logical error rate. Notably, at this error probability, only surface and gross code remain effective.

Analysis. We repeat the experiment at two additional error probabilities, 0.002 and 0.008, to examine whether the effect persists closer to and farther from the codes' thresholds. Across all four

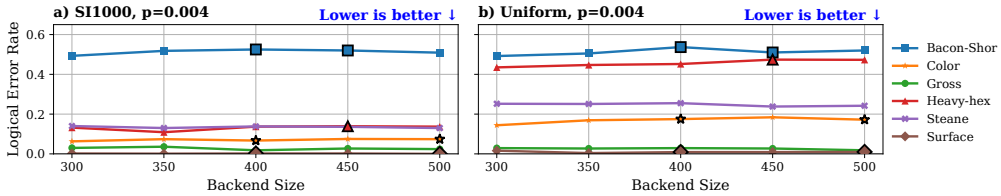


Fig. 9. Logical error rates of different QEC codes at the maximal available code distance across backend sizes under two noise models of error probability 0.004. *Highlighted points mark an increase in the maximal achievable code distance.*

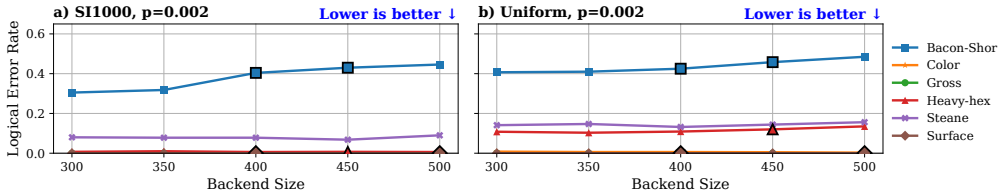


Fig. 10. Logical error rates of different QEC codes at the maximal available code distance across backend sizes under two noise models of error probability 0.002. *Highlighted points mark an increase in the maximal achievable code distance.*

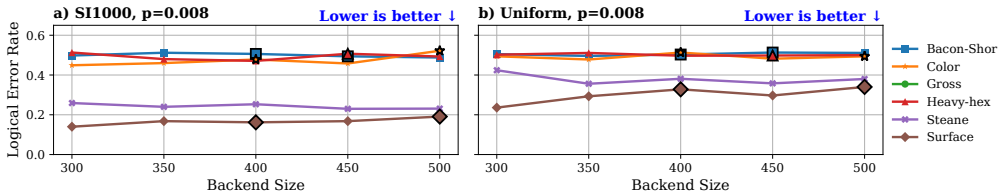


Fig. 11. Logical error rates of different QEC codes at the maximal available code distance across backend sizes under two noise models of error probability 0.008. *Highlighted points mark an increase in the maximal achievable code distance.*

codes and both probabilities, distance variations rarely coincide with the largest deviations from the mean, confirming no consistent trend. At 0.002, all codes except Bacon-Shor perform better, achieving logical error rates of at most 0.156. Color code and gross code produce almost error rate near zero, for surface code we observe no errors. At 0.008, performance degrades across all codes; surface code holds up best under both models, though its logical error rate still exceeds 10%.

Takeaway #1: Our experiments show that increasing code distance does not consistently improve logical performance. The change, on average, raises logical error rates by around 0.012 due to the overhead of additional qubits and gates. This suggests that once a code shows effectiveness, we can use the available device scale to run larger protected circuits instead of raising the distance, enabling more complex algorithms on mid-term hardware.

4.2 Topology Connectivity

Qubit connectivity is a critical factor for QEC because certain hardware topologies (e.g., superconducting) require noisy SWAP gates for routing, which significantly increases error rates [93]. For instance, Figure 12 shows that mapping the Steane code to sparse topologies such as grids or cubes requires additional, error-inducing SWAP gates, an overhead that a fully connected architecture entirely avoids.

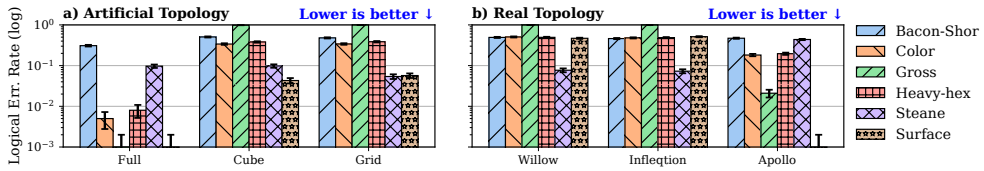


Fig. 13. Logical error rates of different QEC codes under the SI1000 noise model across topologies with varying connectivity. *a) Artificial topologies of 300 qubits with different connectivities and error probability 0.002. b) Realistic topologies with error probability 0.004.*

Research question and hypothesis. These observations raise the following question: **RQ# 2**: *Does higher qubit connectivity always improve the effectiveness of QEC codes?* We hypothesize that higher qubit connectivity reduces SWAP overheads: while a Steane code circuit requires only 49 two-qubit gates on a fully connected device, mapping it to sparser topologies with the Qiskit transpiler [109] adds 54 extra CNOTs on a cube layout and 75 on a grid layout. Since two-qubit gates are a dominant error source [2, 3, 104], this routing overhead will degrade code performance.

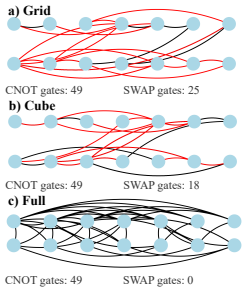


Fig. 12. Connectivity graphs of Steane code $[[7, 1, 3]]$ circuit. *Circuit mapped and routed to various topologies. Black links indicate CNOT connections; red links indicate SWAP connections. Overlapping connections prioritize the noisier SWAP.*

Methodology. To isolate and quantify the impact of connectivity, we simulate each QEC code at its maximum feasible distance on three artificial 300-qubit topologies: a 15×20 grid, a 5×6×10 cuboid, and a fully connected graph. To minimize confounding effects from noise, we use an SI1000 model with a low error probability of 0.002.

Results. The logical error rates, summarized in Fig. 13(a), reveal two distinct trends. First, transitioning from a 2D grid to a 3D cuboid topology yields inconsistent benefits; while the surface code improves by 24.56%, the concatenated Steane performs 81.48% worse. In contrast, adopting a fully connected topology yields substantial and universal improvements, reducing logical errors by an average of 81.92% from a grid. Notably, under full connectivity, we observe no errors for the surface code and the gross code.

Analysis. To validate our findings on realistic hardware, we simulate performance on Google Willow, Quantinuum Apollo, and Infleqtion topologies. Using an SI1000 noise model with a two-qubit error probability of 0.004, the results in Fig. 13(b) confirm that connectivity remains the dominant factor. Apollo, which supports shuttling, achieves an average logical error rate of 0.22, compared to 0.40 on more constrained layouts. The concatenated Steane code delivers the best overall performance with an average error of 0.13; however, we observe only a single error on the surface code on Apollo. Topology dependence is most evident in the gross code: it performs well on Apollo (0.021) but fails on the other platforms.

Takeaway #2: We confirm that connectivity is a crucial factor in the effectiveness of QEC. While transitioning from a 2D grid to a 3D cuboid topology offers inconsistent benefits, moving to an idealized fully connected layout is highly effective, reducing the logical error rate by 81.92% on average. However, such fully connected topologies are physically unrealistic for superconducting qubits due to frequency collisions and crosstalk [138]. Hence, realistic architectures rely on partial-connectivity mechanisms, such as qubit shuttling, which approximate full connectivity over time at the cost of additional latency and noise from qubit movement. With realistic device models, we observe that shuttle capabilities improve performance by an average of 45%. We find that codes exhibit varying sensitivity to these constraints and confirm that high connectivity is essential to unlock the full potential of QEC.

4.3 Variance of Qubit Error Probabilities

We next investigate the impact of non-uniform physical qubit quality on QEC performance. While qubits in trapped-ion and neutral atoms systems are largely uniform [28, 115], superconducting qubits exhibit significant heterogeneity in their decoherence (T_1) and dephasing (T_2) times [125] as well as their readout errors rates [124]. Consequently, relying on device-wide average error rates can be misleading, as a code's performance may be dictated by the specific, lower-quality qubits on which it is executed.

Fig. 14 illustrates T_2 and gate lengths on IBM Heron's `ibm_pittsburgh` [70]. We consider T_2 because it is shorter than T_1. The mean T_2 is 330.14 μs and the median 336.16 μs. However, with the standard deviation of 142.84 μs, there are also qubits of significantly lower lifetimes.

Research question and hypothesis. We raise a question **RQ# 3**: *Is mean qubit quality enough to characterize expected error rates in heterogeneous qubit devices, or does variance also play a critical role?* We hypothesize that reducing the qubit quality variance improves QEC performance by making error patterns more predictable. We show four possible mappings of a distance-3 surface code onto the `ibm_pittsburgh` device in Fig. 14. The choice of physical qubits significantly impacts the average lifetime of the logical qubit; the mean T_2 times for the mappings are 253.00 μs, 355.88 μs, 292.45 μs, and 373.63 μs.

Methodology. We simulate the QEC codes on a 399-qubit all-to-all topology using the IBM Heron noise model to isolate the effects of qubit variability from device size and connectivity constraints. Qubit quality is modeled by sampling T_1 and T_2 values from normal distributions calibrated to IBM Heron data. We explore three variance regimes with standard deviations of 0 μs (none), 60 μs (low), 120 μs (medium), and 180 μs (high), and additionally consider a tenfold prolongation of T_1 and T_2 to study the codes under reduced-noise conditions.

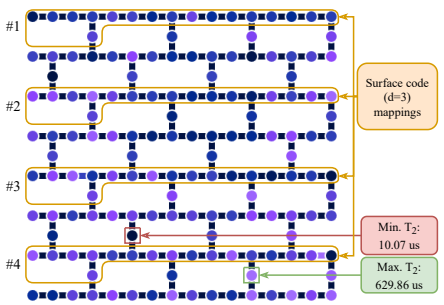


Fig. 14. Qubit topology of the IBM Heron r3 `ibm_pittsburgh` QPU. *Topology of the* `ibm_pittsburgh` *device with qubit* T_2 *dephasing times (μs) shown by color intensity, based on the calibration of 2025-08-29, 07:56:08 [70]. Example mappings of a distance-3 surface code are highlighted with orange frames.*

Results. Fig. 15(a) shows that increasing qubit lifetime variance does not systematically affect logical error rates, with most codes varying by less than 9%. To verify that this lack of correlation is not due to codes being already ineffective under baseline noise, we repeat the simulations with T_1 and T_2 values scaled tenfold to reduce noise, as shown in Fig. 15(b). Even in this high-qubit-lifetime regime, no consistent trend emerges: logical error rates fluctuate non-monotonically, with pronounced oscillations, e.g., the color code's error decreases by 69.64% from mid to high variance.

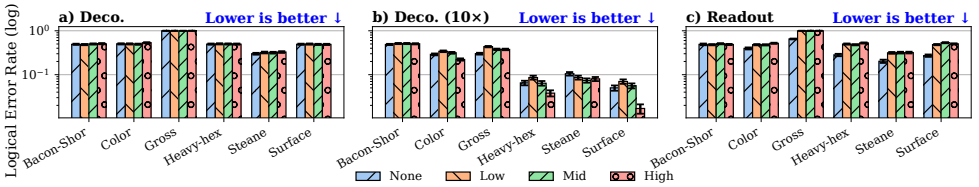


Fig. 15. Influence of qubit quality and readout error variability on the QEC codes. *Comparison of logical error rates on an all-to-all topology for: (a) realistic qubit T_1 and T_2 sampled from normal distributions based on IBM Heron parameters at various variance levels, (b) tenfold prolonged T_1 and T_2, and (c) measurement errors with varying variance from IBM Heron.*

Analysis. However, these results may stem from the relatively small overall influence of decoherence errors. To further explore this effect, we investigate the impact of varying readout errors, another commonly fluctuating source of noise. We model the readout errors using a logarithmic distribution with standard deviations of 0.0, 0.4, 0.7, and 1.0, chosen to best represent the spread of errors observed on the IBM Torino device. As shown in Fig. 15(c), we again observe no clear correlation, with only the Steane code displaying a steady increase in logical error rates across the variation levels (from 0.30 to 0.319).

Takeaway #3: We show that variations in qubit lifetime and readout error do not systematically affect the performance of QEC codes: no consistent correlation is observed, and the average magnitude of differences is 0.02. This is consistent with an important feature of many QEC codes, particularly topological codes as discussed in §3.2, i.e., an immunity to local errors. As long as individual qubits remain below the code's error threshold, local variations in qubit quality have a negligible impact. Our study suggests that incorporating qubit-variance-aware or readout-variance-aware code selection and mapping is unnecessary, which can simplify compiler design.

4.4 Distributed Topology

Next, we explore the effectiveness of QEC codes on distributed devices. Due to scalability limitations of monolithic QPUs, several companies are developing architectures in which multiple QPUs are connected via noisier and slower long-range couplers [107, 117]. For instance, IBM Flamingo consists of three connected IBM Heron QPUs, as we show in Fig. 16. The two-qubit gate error rate for inter-QPU connections is $\sim 10\times$ higher than an intra-QPU connection.

Since the code distance determines the number of corrections [112], we might expect that increasing the distance across distributed QPUs should enhance fault tolerance. However, our study in § 4.1, combined with the noisy nature of inter-QPU connections, challenges this intuition.

Research question and hypothesis. Our next question is **RQ#4:** *Does the effectiveness of a QEC code scale across the QPUs of a distributed architecture similar to when the code runs on a single QPU?* Our results in § 4.3 hint that distributing a QEC code across QPUs will not degrade its performance. We motivate this in Fig. 16, where we scale a surface code from distance $d=3$ on a single 20-qubit QPU to $d=5$ across QPUs, which requires using a few, noisier inter-QPU links. We treat them as high-error outliers, analogous to the low-quality qubits in our previous study, and thus predict that their impact on the logical error rate will be limited.

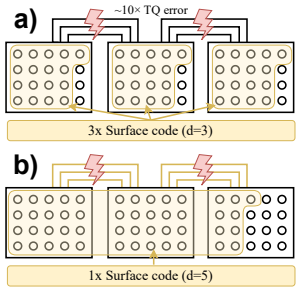


Fig. 16. QEC code placement on a distributed device. *(a) Surface code (d=3) circuits on individual QPUs. (b) Surface code (d=5) circuit spanning the full device.*

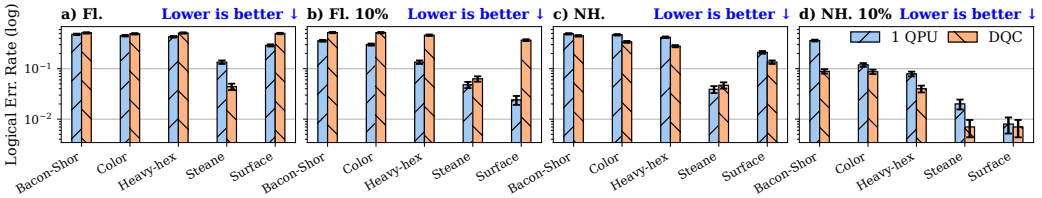


Fig. 17. Performance of QEC codes on a single QPU vs. on the entire DQC architecture of IBM Flamingo (Fl.) and IBM Nighthawk (NH.) with original and tenfold downscaled noise.

Methodology. We test whether this intuition holds on the real-life IBM Flamingo topology. To do so, we compare logical error rates achieved by the QEC codes with their maximal possible distance and with distance limited by the size of a single QPU.

Results. In Fig. 17(a), we compare logical error rates for codes executed on a single QPU versus across the full distributed topology (the gross code cannot be run on a single QPU due to its size, so we exclude it). Single-QPU execution performs substantially better, with an average improvement of 13.27%. The surface code benefits the most (41.88%), while the concatenated Steane code is the only code that performs better on the distributed topology, since its effective distance remains unchanged. Because high error rates render most codes ineffective, Fig. 17(b) shows the same comparison under the IBM Flamingo noise model with error rates reduced by a factor of 10. Here, the single-QPU advantage grows to 55.15%, with the surface code again gaining the most (88.63%) and the concatenated Steane code the least (23.81%). These results suggest that limited inter-QPU connectivity, rather than noise levels, primarily drives the performance gap.

Analysis. To test the role of connectivity, we explore the performance on IBM Nighthawk [108], which has the same error rates as Flamingo but higher connectivity (six neighbors per qubit) and the same quality of inter- and intra-QPU couplers. In Fig. 17(c), only the Steane code performs better on a single QPU under normal noise, and under scaled noise (Fig. 17(d)), no code does. All other codes benefit slightly from the larger distributed system, with average gains of just 0.076 (normal) and 0.072 (scaled).

Takeaway #4: We find that QEC codes on a single QPU perform 34.21% better on average than on distributed QPUs with limited inter-QPU connectivity. Our results show that both stronger and more numerous inter-QPU couplers are critical for achieving fault tolerance in distributed architectures.

4.5 Quantum Technologies

To conclude hardware analysis, we investigate how different quantum technologies support the use of QEC codes on mid-term devices. Since each technology realizes qubits in a distinct way, this leads to heterogeneous noise models, gate speeds, and coherence times (§ 2), as shown in Fig. 18.

Research question and hypothesis. This leads us to ask **RQ#5:** *Which quantum technologies are most suitable for effective error correction, given their error rates and hardware restrictions?* We hypothesize that QEC codes are most effective on platforms

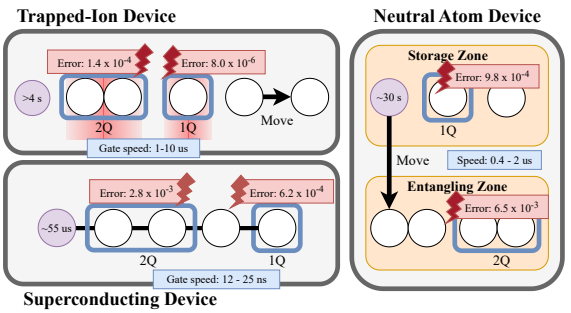


Fig. 18. Overview of quantum technologies. *Gate error rates, coherence times, and gate speeds based on Tab. 1.*

that support shuttling, since enhanced connectivity plays a decisive role in error correction performance as we show in § 4.2. Among these, trapped-ion devices appear particularly promising due to their long coherence times. However, noise rates in realistic mid-term hardware remain above most QEC thresholds, limiting the potential for full fault tolerance. Trapped-ion and neutral atom QPUs support mid-circuit movement and offer a higher ratio of gate speed to coherence time, while superconducting and neutral atoms devices show similar two-qubit error rates, with trapped-ion systems providing an order-of-magnitude improvement. Thus, we expect the mid-term noise levels to be too high for effective QEC.

Methodology. We simulate QEC codes at the maximum distance on mid-term devices for each technology: Google Willow, Quantinuum Apollo, and Infleqtion. We use noise models that capture their corresponding error rates. For devices supporting shuttling, we compare performance with and without it.

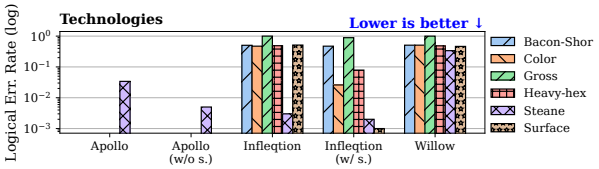


Fig. 19. Effectiveness of codes on realistic mid-term devices, both w/ and w/o mid-circuit qubit movement.

Results. Fig. 19 shows the logical error rate results. Quantinuum Apollo performs best, with average rates of 0.833×10^{-3} without shuttling and 5.67×10^{-3} with, followed by Infleqtion at 4.97×10^{-1} without shuttling and 2.45×10^{-1} with. The gross code fails in all cases except Apollo, where high connectivity and low error rates enable full error suppression. Across technologies, the concatenated Steane code performs best on average (1.11×10^{-1}), although we still observed some errors on Apollo, likely due to the chosen concatenation level. For Apollo, only the concatenated Steane code degrades with shuttling, while all other codes maintain complete reduction. On average, shuttling improves performance from about 0.249 to 0.125, nearly halving the error rate. Projected trapped-ion error rates appear sufficient for practical QEC, as most codes eliminate logical errors on Apollo. On Infleqtion with shuttling, the surface code reaches 1.0×10^{-3}. Although current superconducting devices perform poorly, Fig. 17 shows that a tenfold reduction in IBM Flamingo's physical error rate enables its surface code to reach 9.0×10^{-3}. Our results indicate that if industry roadmaps [105, 107] are met, fault tolerance may be achievable within five years.

Takeaway #5: We observe that shuttling can nearly halve logical error rates. Among the platforms we study, Quantinuum Apollo (trapped-ion) performs the best, often presenting no errors in the sample, while on Infleqtion with shuttling, the surface code brings the logical error rate down to 1.0×10^{-3}. Our results hint that future low-error, high-connectivity hardware will enable near-complete error suppression, putting fault-tolerant QEC within reach.

5 Framework Analysis

In this section, we analyze how certain compilation stages, such as mapping and routing (§ 5.1) and translation to the target gate set (§ 5.2), affect the effectiveness of the protection offered by the chosen QEC codes. Here, we aim to provide insights into the error overhead that must be accounted for when selecting a QEC code for a QPU with a specific noise model and available compiler.

5.1 Mapping and Routing

We investigate the impact of mapping and routing on QEC codes' performance, since these compilation stages substantially increase the number of noisy two-qubit gates [93]. Fig. 20 shows this,

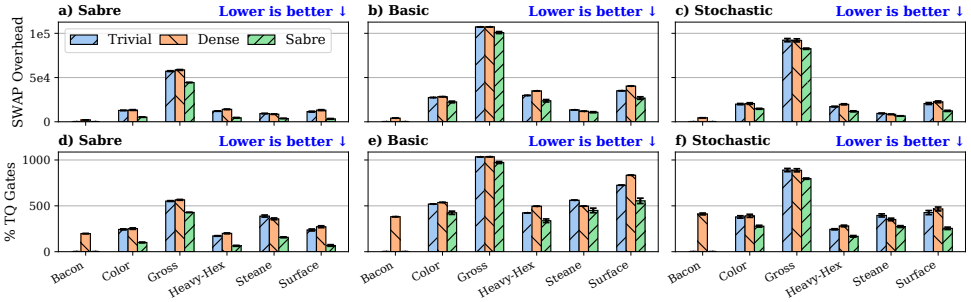


Fig. 21. SWAP overhead (a-c) and SWAP overhead as percentage of original two-qubit gates (d-f) introduced for different QEC codes and routing methods on grid architecture.

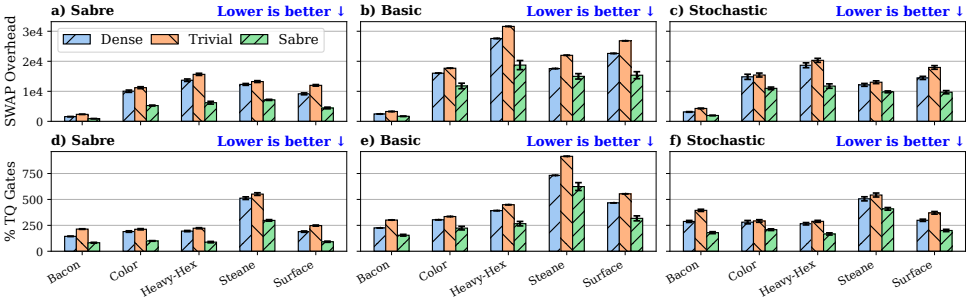


Fig. 22. SWAP overhead (a-c) and SWAP overhead as percentage of original two-qubit gates (d-f) introduced for different QEC codes and routing methods on heavy-hex architecture.

where we map a circuit on a grid topology (a-b). The routing step that follows the mapping adds SWAP gates to resolve the connectivity constraints of the topology (c).

Research question and hypothesis. This motivates the research question: **RQ#6:** *How do the mapping and routing compilation stages influence the effectiveness of QEC codes?* We hypothesize that when mapping and routing heuristics limit SWAP overheads, QEC effectiveness increases. Since many quantum devices do not support SWAPs natively [2, 104], a SWAP is decomposed into three two-qubit gates, effectively tripling the error probability (Fig. 20(c)).

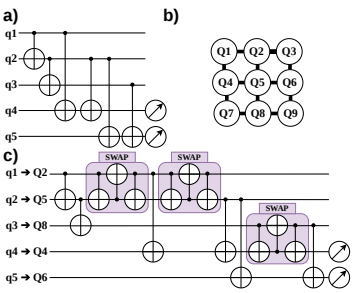


Fig. 20. Circuit mapping and routing on an exemplary topology. *(a) Repetition code (d=3) (b) Grid topology (c) Exemplary mapping of logical to physical qubit, which necessitates additional SWAP gates.*

Methodology. We compile each code 1000 times using all combinations of initial layout strategies and routing heuristics onto a 17×17 grid and the 193-qubit heavy-hex topology, where the gross code is excluded due to prohibitive runtime.

Results. Figures 21(a–c) and 22(a–c) show the SWAP overheads. We exclude the Lookahead mapping from our experiments due to its prohibitively long execution times on larger circuits and topologies. Across all codes, we find that SABRE yields the best results. On average, it introduces 10216.480 SWAP gates per code for grid topology, ranging from 0 for the Bacon–Shor code to 44415.49 for the gross code, and 4789.2756 SWAP gates per code for heavy-hex topology, ranging from 892.139 for the Bacon–Shor code to 7147.208 for the concatenated Steane code. However, even codes typically well-suited for the given topologies, such as the surface code for the grid or the heavy-hex code for the heavy-hex topology, accumulate substantial overhead (3288.283

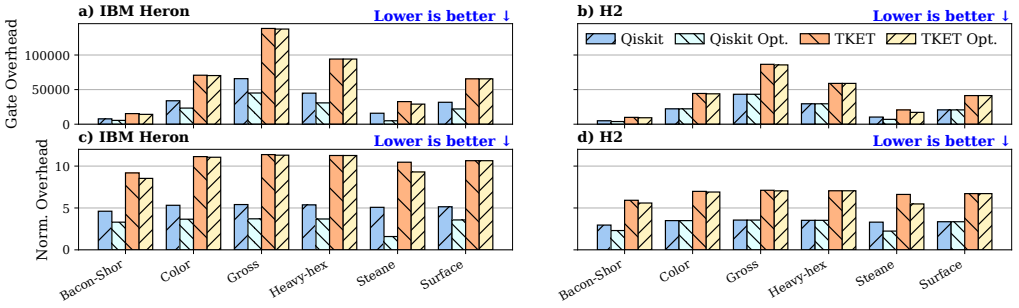


Fig. 24. Gate overhead of converting to IBM Heron and Quantinuum H2 gate sets using TKET and Qiskit.

and 6201.596 additional SWAPs, respectively). Notably, the overhead does not seem consistently proportional across all the codes.

Analysis. Next, we examine how SWAP overhead relates to the number of two-qubit gates in the original circuit, which we show in Figures 21(d–f) and 22(d–f). For the grid topology, SABRE incurs an average overhead of 136.34%, reaching up to 428.39% for the gross code. For the heavy-hex topology, SWAP overhead is around 131.85%. Lastly, we observe that even for codes with similar connectivity needs, the proportions differ significantly. Because of the SWAP decomposition, in fact, we observe an average increase equivalent to 409.02% and 395.55% of the original two-qubit gates, respectively.

Takeaway #6: We show that mapping and routing add 134.095% more two-qubit gates due to SWAP overhead, on average. In practical applications, this corresponds to just over four extra two-qubit gates for every original one, which greatly amplifies two-qubit errors and highlights the need for mapping and routing strategies tailored to QEC to preserve fault tolerance.

5.2 Gateset Translation

We next analyze the error overhead introduced when translating a quantum circuit into a device's native gate set. Each quantum device supports a specific, restrictive set of hardware-level gates [2, 104], requiring compilers to decompose high-level operations into hardware-compliant sequences. Fig. 23 illustrates this process, showing the decomposition required to implement a CNOT gate on a device that does not support it [2].

Research question and hypothesis. This raises a question: **RQ#7:** *How does the translation stage influence the effectiveness of QEC codes?* We hypothesize that different compilers generate hardware-level gate sequences with varying overheads. To illustrate our hypothesis, we consider the example in Fig. 23. The same high-level circuit can be translated in multiple equivalent ways, including with or without optimization. These choices yield different numbers of gates, each contributing to the total error probability.

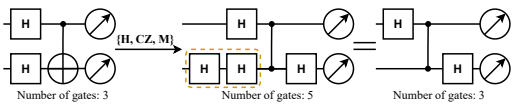


Fig. 23. Example of circuit translation. *Non-optimal and optimal translation into a gate set w/o a CNOT gate.*

Methodology. We compare the number of additional gates introduced when translating each QEC code with maximal distance to the gate sets of IBM Heron and Quantinuum H2 devices. To remove any connectivity constraints, we use a fully connected topology of 300 qubits.

Results. We exclude BQSKit from our results since it removes operations deemed redundant, which interferes with error detection. In Fig. 24(a-b), we show the number of additional gates introduced

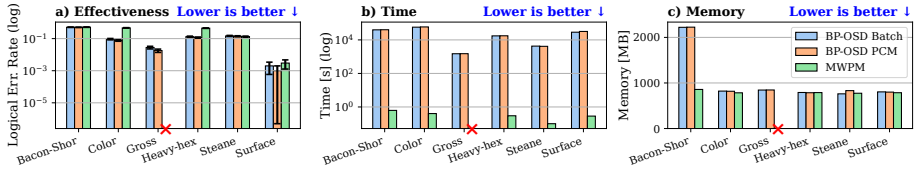


Fig. 26. Comparison of decoders. *a) Effectiveness against the SI1000 noise model with probability 0.004. b) Runtime of the decoders. c) Memory usage of the decoders.*

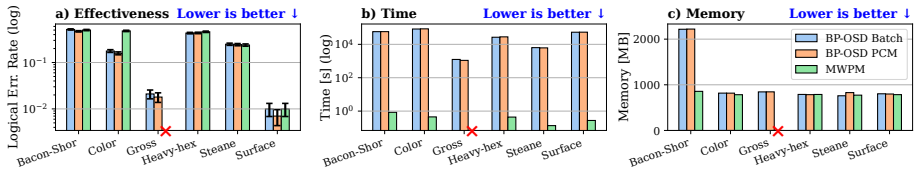


Fig. 27. Comparison of decoders. *a) Effectiveness of different decoders against the uniform noise model with probability 0.004. b) Runtime of the decoders. c) Memory usage of the decoders.*

by translation. The gross code exhibits the highest absolute increase due to its large number of gates. On average, Qiskit introduces 27552 additional gates, while TKET adds over twice as many. At their highest optimization levels, Qiskit reduces the overhead by 21.94%, while TKET at its highest viable level (L2 [103]) achieves just 1.7%. These results demonstrate that optimization mitigates, but cannot fully eliminate, the cost of translation.

Analysis. We investigate whether the overhead is not always proportional to the original gate count. In Fig. 24(c-d), we show that, in contrast to routing, translation overhead scales approximately proportionally with the original gate count. Across all compilers and codes, an average of 6.134 additional gates is introduced per original gate, with TKET contributing 8.704, optimized TKET 8.406, Qiskit 4.261, and optimized Qiskit 3.166. We observe the highest deviation from the average in the Bacon-Shor code, with a normalized overhead of 5.301. This suggests that the majority of codes have similar distributions of gate types, leading to consistent translation scaling.

Takeaway #7: Our investigation shows that even the most optimized translation introduces significant overhead, with an average of 3.166 additional two-qubit gates per original gate. This highlights that, compared to unoptimized circuits, careful compilation is crucial to minimize overhead and limit error accumulation, thereby preserving the effectiveness of QEC codes.

6 Quantum Error Correction Analysis

Finally, we explore the correcting abilities of decoders (§ 6.1) and QEC codes (§ 6.2) themselves.

6.1 Decoders

We examine how the choice of decoder shapes QEC performance, as these algorithms interpret syndrome measurements, predict errors, and propose corrections, with varying accuracy and efficiency [16, 92] (Fig. 25).

Research question and hypothesis. This leads us to raise a question **RQ#8**: *Which decoders achieve the best performance across QEC code families?* We hypothesize that no single decoder consistently dominates, as performance depends on code structure and error propagation.

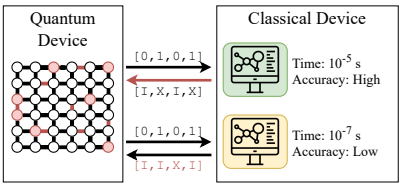


Fig. 25. Decoding algorithms demonstrate a trade-off between speed and accuracy.

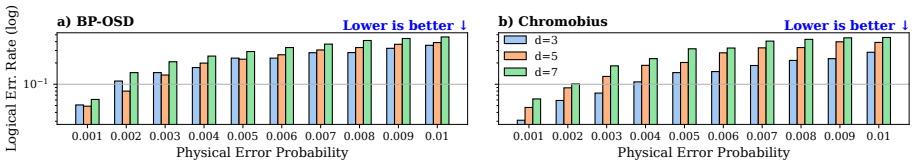


Fig. 28. Difference in logical error rate between BP-OSD and Chromobius for color codes of various distances under the SI1000 error model.

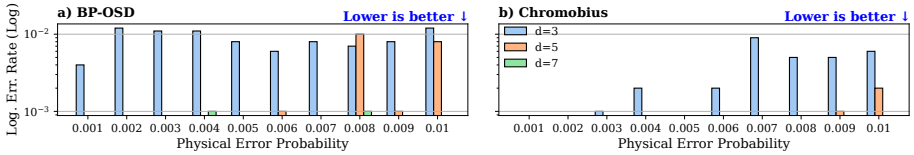


Fig. 29. Difference in logical error rate between BP-OSD and Chromobius for color codes of various distances under the phenomenological error model.

Methodology. We evaluate two open-source decoders: *BP-OSD* [113] and *MWPM* [64], across multiple QEC codes under the SI1000 and the uniform error models ($p = 0.004$). BP-OSD is tested in two variants: parity-check matrix decoding and batched error decoding. In both cases, we use minimum-sum belief propagation with up to 10000 iterations for improved convergence, followed by order-7 OSD, trading increased accuracy for higher computational cost. Each configuration runs on a fully connected 400-qubit topology, using the maximum achievable code distance for each QEC scheme.

Results. Excluding the gross code, for which MWPM fails, the BP-OSD parity-check decoder achieves the best overall performance against the SI1000 noise model across the tested QEC codes, with an average logical error rate of 0.168, outperforming MWPM by 46.66% on average (Fig. 26). MWPM outperforms BP-OSD only for the concatenated Steane code. However, this improved accuracy comes at a substantial computational cost: MWPM requires, on average, only 0.34 s per experiment, whereas BP-OSD requires over 8 h, and MWPM uses 26.89% less memory than the heavier parity-check BP-OSD implementation. Fig. 27 presents the results for the uniform noise model. Here, on average, the BP-OSD decoder with a parity-check matrix achieves the best overall performance across all tested QEC codes, yielding an average logical error rate of 0.2624. It outperforms BP-OSD batch (0.2764) and MWPM (0.3378). Again, the average execution time for BP-OSD algorithms is over 10^5 times longer, while the memory usage is 26.86% smaller for the MWPM than for the less resource-efficient BP-OSD with a parity-check matrix. These results reflect the choice of aggressive BP-OSD settings optimized for decoding accuracy. Reducing the number of BP iterations or the OSD order would significantly shorten the runtime at the expense of performance.

Analysis. General-purpose decoders are essential for cross-code benchmarking but may underperform compared to specialized decoders. We compare the performance of the BP-OSD batch and *Chromobius* [53] decoder tailored for the color code, at distances 3, 5, and 7. Under the SI1000 noise model, Chromobius achieves an average logical error of 0.228 versus BP-OSD's 0.289 (Fig. 28), showing an advantage, but smaller than we anticipated. We further compare the performance of the color code using Chromobius and BP-OSD under a standard, albeit less realistic, phenomenological noise regime, where only noise sources are the depolarization of data qubits between rounds and imperfect measurements [53]. In Fig. 29, we show that under this noise model, Chromobius achieves an average logical error rate of 0.0011, performing approximately 3.3× better than BP-OSD.

Table 5. Observed increase in logical error rate due to decoding.

QEC Code	Bacon–Shor				Heavy–Hex		Con. Steane	
Error prob.	0.004	0.006	0.008	0.010	0.008	0.010	0.001	0.008
ΔLER = Corrected − Uncorrected	+0.003	+0.002	+0.004	+0.005	+0.016	+0.010	+0.014	+0.012

Takeaway #8: BP-OSD achieves the best general decoding performance and, on color code under a realistic noise model, performs only 26.75% worse than a dedicated decoder, making it the most suitable choice for cross-code evaluations.

6.2 Is QEC Essential for Quantum Computing?

We close with a provocative question: is QEC always necessary? Here, we examine errors introduced by the correction procedure itself, highlighting the gap between ideal fault-tolerance and the reality of QPUs suffering from various noise sources (Fig. 30).

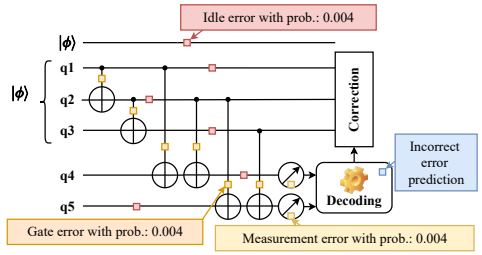


Fig. 30. Example of errors in an unprotected versus a protected qubit. *Comparison of errors in quantum memory w/o protection and w/ a repetition code under an uniform noise model.*

Research question and hypothesis. Thus, we ask: **RQ#9:** *Is the application of QEC always beneficial, or are there regimes in which the overhead of QEC introduces more noise than it suppresses?* We hypothesize that applying QEC can be detrimental as the error probability approaches a code's threshold. Consider a single idle qubit with error probability p_{idle}. Protecting it with a simple repetition code (Fig. 30) introduces additional errors from gates (p_{gate}) and measurements (p_{meas}), yielding a combined error probability of approximately $5 \times p_{idle} + 6 \times p_{gate} + 2 \times p_{meas}$. Once the code's correcting capabilities are exceeded, the correction process itself becomes a net source of faults, making the encoded qubit noisier than the unprotected one. We aim to investigate whether, across different error probabilities and especially near the threshold, this extra overhead causes the logical error rate to grow faster than that of the unprotected qubit.

Methodology. We compare error growth in protected and unprotected circuits by generating the QEC codes at maximal distance, on a fully connected 300-qubit topology, and their corresponding unprotected circuits, consisting of a single idle qubit (12 for the gross code), which we keep idle for as many rounds as their protected counterparts. We add noise using the SI1000 model with two-qubit error probabilities in the 0.001–0.01 range, and record the resulting error rates.

Results. We observe no errors on unprotected qubits at any probability. We present results for protected circuits in Fig. 31. At $p = 0.001$, we observe errors for two codes. At $p = 0.004$, all codes exceed their thresholds. Surface code exhibits the slowest error growth, while the gross code, with the most gates, deteriorates most sharply. We expect that in more constrained topologies, the higher gate count will result in even faster performance degradation.

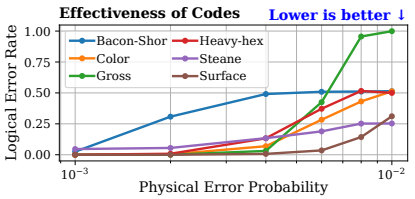


Fig. 31. Logical error rates for different codes under the SI1000 noise model of various probabilities in a realistic setup.

Analysis. To further investigate the introduced overhead, we also isolate the effect of the correction itself. As expected, logical error rates are almost always higher without correction, even after a code's threshold is crossed, confirming the codes' error-suppressing capabilities. However, as shown in Tab. 5, this benefit is not universal: in some cases, incorrect decoder decisions actively degrade performance rather than improve it.

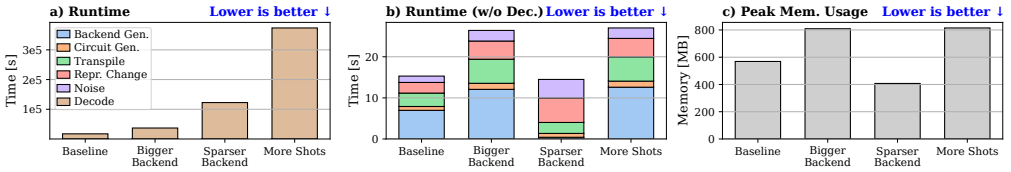


Fig. 32. Runtime per stage and peak memory usage of ECCentric. *Baseline: Running surface code on a fully connected 300-qubit backend (SI1000 noise, error 0.004) with BP-OSD decoder for 1000 shots. Bigger backend: 400 qubits. Sparser backend: grid topology. More shots: 10000 shots.*

Takeaway #9: Our study shows that QEC is not universally beneficial. At $p = 0.001$, we observe no errors only on four of the evaluated codes, and at $p = 0.004$ all codes cross their thresholds, while unprotected qubits still show no observed errors. Although QEC can suppress errors at low rates, once a code's threshold is crossed, its performance deteriorates rapidly, depending on its correcting capabilities and the noise sources in the circuit. These results suggest that QEC should be applied selectively, only where error rates are low or to protect complex circuits rather than quantum memory, to achieve meaningful error suppression.

7 Limitations

ECCentric implementation. Our implementation does not include FT gate constructions, as no general, scalable framework exists across different QEC codes, and practical methods to enable FT gates are still an active area of research aimed at reducing overhead. Once such methods become available, ECCentric will support circuits in this more general FT setting. We also omit realistic decoding delays, since latency depends strongly on the QEC code, decoder, and hardware, making general comparisons difficult. Although we could assume optimistic sub-microsecond latencies, they would have minimal impact and risk introducing code- or hardware-specific bias. Future versions of ECCentric may offer configurable latency models.

ECCentric execution. ECCentric supports exact sampling of QEC-protected quantum memory circuits, but at significant memory and runtime cost. Fig. 32 shows that the decoding stage, during which errors are sampled via stabilizer simulation and a decoding heuristic is applied, dominates runtime, accounting for an average of 99.96% of runtime, as errors are sampled via stabilizer simulation and processed by a decoding heuristic. Since Stim can simulate a surface code ($d = 100$) in 15 s [52], decoding becomes the bottleneck as detection events increase with code distance and additional gates for sparse backends, with shot count determining total runtime. Memory usage remains consistent across execution stages and scales with backend size, connectivity, and shots, reaching up to 815 MB per experiment. Overall, ECCentric execution is constrained by both memory and runtime, which can extend over multiple days.

8 Related Work

Benchmarking in quantum computing. Recent comprehensive surveys [91, 102] highlight the crucial role of benchmarking in guiding the development of the entire quantum computing stack. Established suites now exist for assessing quantum software [87, 110, 126], development kits [97], and physical qubit performance [95]. However, these existing benchmarking studies are QEC-agnostic and thus orthogonal to our work.

Benchmarking in QEC. While systematic evaluations of QEC codes are scarce, existing studies tend to be limited in scope. Much of the prior work focuses on specific QEC-related aspects [29, 82, 123, 128, 136, 139], relies on theoretical analysis with simplified noise models [14, 23, 24, 35, 36, 54, 67, 122], or tests only a single code, topology, or noise model under realistic conditions

[17, 32, 37, 43, 60, 72, 127]. Furthermore, evaluations on real hardware remain rare [45, 69]. In contrast, our work bridges this gap by systematically benchmarking a wide range of QEC codes under realistic, device-specific noise models, while accounting for compilation effects to deliver a comprehensive evaluation of their practical applicability.

Existing frameworks. While several QEC benchmarking frameworks exist, they are often limited. The most established is Stim [49], which enables efficient stabilizer simulations but offers only simple noise models out of the box. Other efforts are either limited in scope [59], deprecated [133], or restricted to specific code families [75, 77]. In contrast, our work builds on Stim's stabilizer simulation to provide a general framework for evaluating a broad spectrum of codes under precise noise models, while incorporating software stack effects and maintaining efficiency.

Surveys. While several surveys of QEC codes exist, they often focus on deep theoretical foundations [47, 74, 94] or target broader audiences [33, 34, 112]. Even the comprehensive Error Correction Zoo [5], a valuable community catalog, uses a non-uniform presentation that hinders direct comparison. In contrast, our work focuses on the practical aspects of QEC and introduces a clear taxonomy designed to highlight the key characteristics and interrelations between different code families, enabling a more direct, comparative analysis.

How our paper differs? This work systematically benchmarks multiple QEC codes with an emphasis on practical application, evaluating them under real devices, compilers, and noise models. To do so, we introduce a framework that integrates diverse codes, architectures, compilers, noise models, and decoders, and is easily extensible as the field evolves. Complementing this, our survey targets a broad audience and introduces a clear taxonomy that highlights code characteristics, overlaps, and differences, clarifying their strengths and constraints.

9 Concluding Remarks

We present a unified benchmarking framework enabling systematic and comprehensive empirical analysis of QEC codes. Our results provide valuable insights into the performance of QEC codes under various hardware- and framework-specific limitations, aiding the pursuit of FT quantum hardware. Future work should investigate factors beyond the scope of this study, including the evaluation of decoders and the translation of quantum circuit gates to their FT counterparts.

Having systematically explored the performance of QEC codes across mid-term devices, topologies, and noise regimes, we now draw practical lessons for hardware design, compilation strategies, and execution of quantum circuits. Our findings highlight which factors matter most for effective error correction and which can be deprioritized.

- **Trapped-ion in the lead:** Predicted trapped-ion devices with shuttling achieve the strongest error suppression, nearly eliminating logical errors. Prioritizing this platform's development is the most direct path to achieving fault-tolerant QEC within five years (**Takeaway #5**).
- **Connectivity outweighs code size:** Enhancing qubit connectivity through features like mid-circuit movement or shuttling dramatically reduces logical errors, proving far more effective than simply increasing code distance (**Takeaways #1, #2, #5**).
- **Variability is less critical:** Variations in qubit or readout quality have minimal impact on logical errors. This suggests that variance-aware mapping or code selection can be de-emphasized, simplifying both compilation and operational planning (**Takeaway #3**).
- **Distributed execution is still challenging:** Single-QPU patches consistently outperform distributed setups due to the limited connectivity of inter-QPU couplers. Increasing the number of links is the key to enabling distributed fault-tolerant QEC (**Takeaway #4**).

- **QEC-aware compilation is crucial:** The compilation process, particularly routing and mapping, can quadruple the two-qubit gate count. QEC-aware compilation is therefore essential to minimize this error-inducing overhead and preserve a code's effectiveness (**Takeaways #6, #7**).
- **QEC is not always helpful:** In our experiments, we found that in regimes where gate errors dominate, applying QEC indiscriminately can actually introduce more errors than it corrects. For near-term devices, this means we need to carefully decide when and where to apply QEC, particularly avoiding protection of idle qubits unless necessary, and focusing on more complex circuits where error correction truly provides a benefit (**Takeaway #9**).

Artifact. ECCentric, along with the entire experimental setup, datasets, and results, is publicly available on Zenodo: https://doi.org/10.5281/zenodo.19241564.

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